REMARKS

Applicants thank the Examiner for the thorough consideration given the present application. Claims 8 and 10-12 are currently being prosecuted. The Examiner is respectfully requested to reconsider his rejections in view of the Amendment and Remarks as set forth below.

Entry of Amendment

It is respectfully requested that the Amendment should be entered into the official file in view of the fact that the Amendments to the Claims automatically place the application in condition for allowance. Alternatively, if the Examiner does not agree that the application is in condition for allowance, it is respectfully requested that the present Amendment should be entered for the purpose of appeal. The current amendments reduce the issues on appeal by specifying the language of the claim to overcome the indefiniteness rejection. Also, one additional word has been added to clarify that the pad is a single pad in order to help overcome the art rejection. Thus, entry of this Amendment reduces the issues on appeal.

Claim Objections

The Examiner objected to claims 8 and 11, and indicated that the reference to the drain regions and the source regions in claims 8 and 11 did not have antecedent basis. Applicant disagrees that antecedent basis is lacking. In each case, the immediately proceeding line provides antecedent basis. Thus, line 13 of claim 8 recites that each of the MOS-FETs has a drain region. The fact that the following line refers to the plural form, "drain regions", relates to the fact that there are more than one MOS-FET as indicated in line 3 of the claim. Thus, since each of the transistors has a drain region, and there is more than one transistor, antecedent basis is provided for in the plural form. However, in order to make this more clear, Applicants are inserting "of the "MOS-FETs" in each of claims 8 and 11 after the recitation of the regions. Applicants submit that this overcomes the indefiniteness.

Rejections under 35 U.S.C. § 103

Claims 8 and 10-12 stand rejected under 35 U.S.C. § 103 as being obvious over Chisiki (U.S. Patent 5,714,796) in view of Igarashi (U.S. Patent 4,656,491) and Steudel (U.S. Patent 3,712,995). This rejection is respectfully traversed.

The Examiner relies on Chisiki to show an ESD protection component having two MOS field effect transistors of a first conductivity type with two gates and formed in parallel on a first semiconductive layer having a second

semiconductivity type, a first well having a first conductivity type formed on the semiconductive layer including the connecting area and a first opening area. Each of the MOS-FETs has a source region of the first conductivity type and the source regions are commonly and directly connected to a power rail. The first well is electrically connected to a pad and the first doping area is directly connected to a pad. Each of the MOS-FETs has a drain region of the first conductivity type and the drain regions are each connected to a pad. The Examiner admits that Chisiki does not show a first well having two parallel extension areas formed perpendicular to the gates of the MOS-FETs.

The Examiner relies on Igarashi to show a first well having two parallel extension areas. The Examiner also relies on Steudel to show a first well with two parallel extension areas. The Examiner feels that it would have been obvious to have a first well having two parallel extension areas in Chisiki's device in order to improve the device characteristics and provide better protection.

In regard to Applicant's earlier arguments that Chisiki does not teach that the drain regions are commonly and directly connected to the same pad, the Examiner argues that the claim does not require that the drain regions be connected to the same pad. Applicants disagree with this understanding as previously presented. The word "commonly" means that the drain regions are all connected to the same point. Also the fact that the article used before "pad" is "a" indicates that a single pad is involved. Accordingly, Applicants submit that the

Examiner's argument is not convincing. However, to further the prosecution, Applicants make this point even clearer by inserting the word "single". Applicants submit that the present recitation cannot be interpreted anyway other than that all the drain regions are connected to the same pad. In view of this, Applicants submit that the Examiner's argument is removed and that accordingly, the rejection is overcome. Accordingly, Applicants submit that claim 8 and dependent claims 10-12 now overcome this rejection.

Further, the Examiner has correlated various regions of the claims with regions in Chisiki. However, as indicated in column 7 of Chisiki, the reverse biased p-n junction between wells 32 and 34 floats the light-doped n-type well 32 such that the P-channel enhancement type FET 26 never turns on. As a result, the complimentary inverter circuit 23 never inverts the output data signal S2. If the drain regions 27b and 29b of the FETs 27 and 29 are connected to the same pad, the complimentary inverter circuit 28 would invert the output data signal S2 because the well region 29 is not disposed and a light-doped n-type well, such as well region 32. Thus, Chisiki teaches drain region 27b and 29b are connected to different pads. Accordingly, Chisiki teaches away from the claimed invention and there is no motivation to connect drain regions of the FETs 27 and 29 to the same pad as is presently claimed.

Accordingly, none of the three cited references teaches that the drains are connected to one pad as is presently recited so that Applicants submit that the claims are allowable.

In regard to claim 10, the claim states that the first doping area is directly connected to the pad. However, in Chisiki, the doped region is not directly connected to the I/O pad (DB) connected to the drain region 27b or the I/O pad (Nout) connected to drain region 29b. Accordingly, Applicants submit that claim 10 is further allowable.

In regard to claim 12, the claim recites that the first well is directly connected to the pad through the extension areas. In the reference, however, the well 33 is not electrically connected to I/O pad (DB) connected with drain region 27b or the I/O pad (Nout) connected with the drain region 29b. Further, in Igarashi, the wells 12 and 31 are not electrically connected to a pad connected with drains of two FETs. Also, in Steudel, the first well 69 is not electrically connected to a pad connected with drains of two FETs. Accordingly, Applicants submit that claim 12 is further allowable.

Conclusion

In view of the above Remarks, it is believed that the claims clearly distinguish over the patents relied on by the Examiner, either alone or in

combination. In view of this, reconsideration of the rejections and allowance of all of the claims is respectfully requested.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Robert F. Gnuse (Reg. No. 27,295) at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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0941-0342P

Attachment(s)